Prior art EEprom devices only allow the voltage supplied to the control gate V_{CG} to assume one of two voltages, namely V_{CC} or the higher programming voltage of about 12V.

In another aspect of the present invention, the voltage supplied to the control gate V_{CG} is allowed to be independently and continuously variable over a wide range of voltages. This is provided by V_{PG} from the controller 1140. In particular V_{CG} in a line 1083 is fed from V_{PG} which is in turn supplied by the controller from a line 1901. Figure 27 shows V_{PG} to assume various voltages under different functions of the EEprom.

The variability of V_{CG} is particularly advantageous in program and erase margining schemes. In program margining, the read during program verify is done with V_{CG} at a slightly higher voltage than the standard V_{CC}. This helps to place the programmed threshold well into the state by programming past the breakpoint threshold level with a slight margin. In erase verify, the cell is verified with a somewhat reduced V_{CG} to put the cell well into the "erased" state. Furthermore, margining can be used to offset the charge retention problem described earlier (Figure 16B).

As mentioned before, prior art EEproms typically employ V_{CC} to feed V_{CG} during program or erase verify. In order to do margining, V_{CC} itself needs to be ramped up or reduced. This practice produces inaccurate results in the reading circuits since they are also driven by V_{CC}.

In the present invention, the variability of V_{CG} independent of voltages supplied to the reading circuit produce more accurate and reliable results.

Furthermore, the wide range of V_{CG} is useful during testing and diagnostic of the EEprom. It allows the full range of the programmed cell's threshold to be measured easily by continuing to increase V_{CG} (up to the maximum limited by the device's junction breakdown).--

IN THE DRAWINGS:

Add the accompanying sheets 6-22 of drawings, in informal form, which contain additional Figures 9-27.

IN THE CLAIMS:

Please cancel the original parent application claims 1-62, without prejudice, and substitute the following new claims therefore:

--63. A circuit for identifying a memory cell having stored therein an incorrect data value, comprising:

a device operable to read said stored data value after a write cycle;

a comparator having a first input coupled to said device and operable to receive said stored data value, having a second input operable to receive a correct value data that was to be stored in said cell during said write cycle, and having a pair of outputs, said comparator operable to generate a first signal on a first of said outputs when said stored data value is unequal to said correct data value and a second signal on said second output in response to said first signal and when said correct data value equals a programmed value.

64. The circuit of claim 63 wherein said device comprises a sense amplifier.

65. The circuit of claim 63 wherein said comparator comprises a storage device coupled to said second input and operable to store said correct data value.

66. A circuit for identifying a memory cell having stored therein an erroneously unprogrammed data value, comprising:

a read device having an input coupled to said memory cell and having an output;

a first signal line that carries a proper data value that was provided to said memory cell for storage;

a second signal line that carries a first signal level if said stored data value equals said proper data value and a second signal level if said stored data value does not equal said proper data value;

a third signal line that carries a third level if said stored data value does not equal said proper data value and said stored data value equals an unprogrammed value; and

a comparator having a first input coupled to said output of said read device, a second input coupled to said first signal line, a first output coupled to said second signal line, and a second output coupled to said third signal line.

67. A method for identifying an erroneous content of a memory cell after writing a data value to said memory cell, comprising:

reading said content;

comparing said content with said data value;

generating a first signal if said content is unequal to said data value; and

generating a second signal if said content is unequal to said data value and if said content should equal a programmed data value.

68. The method of claim 67 further comprising programming said memory cell in response to said second signal.